REMARKS

Claims 8 and 9 are amended, claims 1-7 are canceled, and no claims are added; as a result, claims 8-30 are now pending in this application.

Affirmation of Election

On January 25, 2005, Examiner Chat C. Do telephoned Applicant's representative J. Michael Anglin to impose a restriction requirement for claims 1-30. Restriction to one of the following claims was required:

Group I: Claims 1-7; or

Group II: Claims 8-30.

Applicant affirms the telephone election to prosecute the invention of Group II, claims 8-30, as provisionally elected without traverse by Applicant's representative, J. Michael Anglin, on January 25, 2005. The claims of the non-elected invention, Group I, claims 1-7, are hereby canceled. Applicant reserves the right to introduce the non-elected claims in one or more divisional applications at a later date.

§102 Rejection of the Claims

Claims 8-9, 15-16, and 19-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by Chip *et al.* (Chip Stearns, *et al.*, *The Coreware Methodology: Building a 200 Mflop Processor in 9 Man Months,* IEEE, 549 (Sept. 1992)). Applicant respectfully traverses the rejections of claims 16 and 19-23.

Claim 8

Claim 8 as amended recites a multiplier coupled to "receive interleaved" operands and to produce a product. Applicant directs the Examiner's attention to the specification of the present application on page 5, lines 25-29, which states,

> As a result, the operands on nodes 217 and 218 are interleaved between the sets $\{A_i, B_i\}$ and $\{C_j, D_j\}$. Multiplier 232 receives the interleaved operands on nodes 217 and 218, multiplies them, and produces a data stream on node 102 interleaved between the products (A_iB_i) and (C_jD_j).

Thus, claim 8 recites a multiplier coupled to receive interleaved operands. In contrast, Chip *et al.* on page 550, right hand column at lines 5-12 recites,

> In this case, shown in Figure 2, a 4-stage pipe exists in both the multiplier and the adder. The pipe stages allow the arithmetic cores to operate on four ordinate transformations in parallel. The floating-point multiplier and adder are effectively interleaved, with each stage transforming one coordinate in the vertex. Table 2 shows how the interleaved scheme transposes the order of the operations to match the latency of the architecture. (emphasis added)

Thus, Chip *et al.* discloses operations on four ordinate transformations in parallel. Further, Figure 2 shows a single operand, χ, being multiplied by four operands, *a*, *e*, *i*, and *m*. In addition, Table 2 of Chip *et al.* shows multiplier operations where clock cycle 1, 2, 3, and 4 involve multiplier operations on $a\chi$, $e\chi$, $i\chi$, and $m\chi$. Thus, four clock cycles in a row involving the operand χ, followed by clock cycles 5, 6, 7, and 8 involving multiplier operations on b*y*, f*y*, j*y*, and n*y*, all including the operand *y*. Hence, Chip *et al.* merely shows operations on a series of operands, first including χ and then *y*, but fails to teach "a multiplier coupled to receive interleaved operands" as recited in amended claim 8. There is no teaching of suggestion in Chip *et al.* that the multiplier in Chip *et al.* receives interleaved operands. Further, "effectively interleaving" the multiplier with the adder using a 4-stage pipe fails to teach a multiplier coupled to "receive" interleaved operands and to produce a product, as recited in claim 4. In addition, the "effective interleaving" described in Chip *et al.* fails to teach the actual interleaving between sets of operands as taught by the present invention and as recited in claim 8.

Therefore, Chip *et al.* fails the teach each of the elements of claim 8 as amended, and so the Office Action fails to state a *prima facie* case of anticipation with respect to claim 8 as amended.

Dependent claims 9 and 15

Claims 9 and 15 depend from claim 8 and therefore include all of the elements of claim 8. For reasons analogous to those stated above and elements in the claims, Chip *et al.* fails to teach each of the elements recited in claims 9 and 15. Therefore, the Office Action fails to state a *prima facie* case of anticipation with respect to claims 9 and 15.

Claim 16

Claim 16 recites, "the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads." As noted above, Chip *et al.* on page 550, in the right hand column at lines 5-7 recites, "in Figure 2, a 4-stage pipe exists in both the multiplier and the adder." However, Chip *et al.* fails to teach the elements of claim 16 as recited above because Chip *et al.* goes on to state on page 550, in the right hand column at lines 7-8, "The pipe stages allow the arithmetic cores to operate on four ordinate transformations in parallel." (emphasis added) Therefore, the four separate registers relied on by the Office Action on page 4 represent registers operating in parallel on four ordinate transformations. Operations in parallel does not teach operations on multiple threads, and thus does not teach "the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads" as recited in claim 16. As argued above with regards to claim 8, Chip *et al.* does not receive interleaved operands at the multiplier. Since Chip *et al.* does not receive interleaved operands (multi-threaded) at the multiplier, Chip *et al.* does not teach the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads, as recited in claim 16.

Therefore, Chip *et al.* fails the teach each of the elements of claim 16, and so the Office Action fails to state a *prima facie* case of anticipation with respect to claim 16.

Dependent claims 19-22

Claims 19-22 depend from claim 16, and therefore include all of the elements of claim 16. For reasons analogous to those stated above and elements in the claims, Chip *et al.* fails to teach each of the elements recited in claims 19-22. Therefore, the Office Action fails to state a *prima facie* case of anticipation with respect to claims 19-22.

Claim 23

Claim 23 recites, "the accumulator including sequential elements to provide a multi-threaded capability." The specification of the present application on page 5 at lines 1-2 states, "Accumulator circuit 100 is a 'multi-threaded' accumulator because it operates on two 'threads' simultaneously" Further, the specification of the present invention on page 5, lines 25-30 states,

> As a result, the operands on nodes 217 and 218 are interleaved between the sets $\{A_i, B_i\}$ and $\{C_j, D_j\}$. Embodiments of the present invention may include more than two threads. For example, the specification on page 5, lines 6-10 states, "In other embodiments, three or more threads are operated on at once. The number of threads that can be operated o simultaneously is a function of the number of partial adders and intermediate registers included in the circuit

In contrast and as noted above, Chip *et al.* discloses, "arithmetic cores to operate on four ordinate transformations in parallel." A disclosure of "parallel" operations fails to teach the multi-thread operations of the present invention. Therefore, and for reasons analogous to those stated above with regards to claim 8, Chip *et al.* fails to teach "the accumulator including sequential elements to provide a multi-threaded capability" as recited in claim 23.

Therefore, Chip *et al.* fails the teach each of the elements of claim 23, and so the Office Action fails to state a *prima facie* case of anticipation with respect to claim 23.

Summary

For at least the reasons stated above, Applicant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 8-9, 15-16, and 19-23.

§*103 Rejection of the Claims*

Claims 10-11

Claims 10-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chip *et al.*

Claims 10-11 depend from claim 8, and therefore include all the elements of claim 8. Claim 8 as amended recites, "a multiplier coupled to receive interleaved operands and to produce a product; and a multi-threaded accumulator coupled to the multiplier to receive the product." As stated in connection with claim 8, Chip *et al.* fails to teach or suggest a multiplier coupled to "receive interleaved operands," and fails to teach or suggest a "multi-threaded" accumulator coupled to the multiplier to receive the product, as recited in claim 8.

The additional cited document Debabrata *et al.* fails to remedy the deficiency. Debabrata *et al.* on page 501 states, "The MAC architecture consists of a multiplier core to produce the products of the two numbers and an accumulator to add together these products." However,

Applicant does not find in Debabrata *et al.* a teaching or suggestion of a multiplier coupled to "receive interleaved operands," or a teaching or suggestion of "multi-threaded accumulator coupled to the multiplier to receive the product," as recited in claim 8. Thus, neither Chip *et al.* nor Debabrata *et al.*, either alone or in combination, teach or suggest all of the elements of claims 10-11, and so the Office Action fails to state a *prima facie* case of obviousness with respect to claims 10-11.

Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Office Action on page 6 states, "it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace the mantissas in carry-save format as seen in Debabrata et al.'s invention into Chip et al.'s invention because it would enable to increase the system performance (e.g. page 502 last two lines and page 503 first two lines)."

Applicant disagrees. The cited portion of Debabrata *et al.* states, "Addition of 2 logical bits of the operand requires a 4 → 2 adder. Hence, the clock period cannot be less than the delay of a 4 → 2 compressor. This will be referred to as a Carry-Save Accumulation (CSA) bottleneck. The CSA bottleneck affects the throughput." Therefore, Debabrate *et al.* is concerned with the Carry-Save Accumulation bottlenecks. The Office Action on page 6 admits that Chip *et al.* fails to disclose "mantissa is in carry-save format." Thus, Chip *et al.* is not concerned with Carry-Save Accumulation, and so the statements in the Office Action for support of the combination of Chip *et al.* with Debabrata *et al.* are not found in the cited documents, and therefore are mere speculation based on the Applicant's disclosure. Because the statements in the Office Action are not supported by the cited documents, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 10-11.

For at least the reasons stated above, Applicant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 10-11.

Claims 12-14, 17-18, and 24-30

Claims 12-14, 17-18, and 24-30 were rejected under 35 U.S.C. § 103(a) as being obvious over Chip *et al.* in view of Choquette (U.S. Pat. No. 6,480,872). Applicant does not admit that

Choquette is prior art and reserves the right, as provided for under 37 C.F.R. 1.131, to "swear behind" Choquette. Applicant respectfully traverses the rejection of claims 17-18 and 24-30.

On pages 7-8, the Office Action repeatedly states that the combination of Chip *et al.* with Choquette would have been obvious because the combination "would enable to properly producing [sic] the correct product-accumulation by shifting or aligning the product to the accumulation register." The Office Action relies on column 5, lines 5-9 of Choquette to support this statement. However, Choquette at column 5, lines 4-9 merely states,

> One of the two operands, commonly the smaller number of the two operands, is passed to the shifter 414 where the operand alignment is performed. Upon proper alignment between the operands, a FP addition is performed in the adder 416 and the result of the addition is stored in the result register 418.

Thus, there is no teaching or suggestion in the cited portion of Choquette to combine the shifter of Choquette with the matrix multiplication based on interleaved multiplier accumulator algorithm of Chip *et al.*, as recited in the Abstract of Chip *et al.* Further, the inference of the statement made in the Office Action is that Chip *et al.* would be unable to produce the "correct" product-accumulation without the shifting of Choquette. However, Chip *et al.* on page 550, right hand column, beginning at line 1 states, "One of the keys to accomplishing the 200 MFlops peak performance is the interleaved Multiplier-Accumulator architecture." Therefore, the inference that Chip *et al.* requires shifting or aligning to produce a "correct" product accumulation appears to be counter to the disclosure in Chip *et al.*

In addition, on page 9 the Office Action states that the combination would have been obvious because it would "enable to properly provide a desire [sic] format as predetermined by the system," and because it would "increase the system performance by bypassing the alignment." Applicant notes that the Office Action fails to point to any portions of either of the cited documents that supports these statements. Because the Office Action fails to show how the suggestion to make the claimed combination and the reasonable expectation of success are found in the cited documents, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 12-14, 17-18, and 24-30.

Further, claims 12-14 depend from claim 8, claims 17-18 depend from claim 16, and claims 24-30 depend from claim 23. Therefore, these dependent claims include all of the

elements of the independent claim from which they depend. For reasons analogous to those argued above, Chip *et al.* fails to teach or suggest each of the elements recited in claims 8, 16, and 23. The additional cited document Choquette fails to remedy the deficiency. Choquette at column 4, lines 52-46 recites, "In operation, the multiply array 410 multiplies operand 1 ("op1") to operand 2 ("op2") from working register A and B as shown in FIG. 4, and passes the result of the multiplication to the first adder 412, the shifter 414, and the result register 418." However, Applicant does not find in Choquette a teaching or suggestion of "interleaved operands" or a "multi-threaded accumulator coupled to the multiplier to receive the product" as recited in claim 8, or a teaching or suggestion of "the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads" as recited in claim 16, or a teaching or suggestion of "the accumulator including sequential elements to provide a multi-threaded capability" as recited in claim 23. Thus, neither Chip *et al.* nor Choquette, either alone or in combination, teach or suggest all of the elements of claims 8, 16, and 23. Therefore, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 12-14, 17-18, and 24-30.

For at least the reasons stated above, Applicant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 12-14, 17-18, and 24-30.

Documents Cited but Not Relied upon for this Office Action

Applicant need not respond to the assertion of pertinence stated for the references cited but not relied upon by the Office Action since these references are not made part of the rejections in this Office Action. Applicant is expressly not admitting to this assertion and reserves the right to address the assertion should it form part of future rejections.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney J. Michael Anglin ((612) 373-6971) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 11 July 2005 By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 11th day of July 2005.

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